AMENDMENTS TO THE CLAIMS

In the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Currently Amended) A decoder circuit mounted on an integrated circuit, the decoder circuit comprising:

a single external input terminal configured to supply an input voltage for decoding by the decoder circuit into three or more control outputs;

a P-type transistor comprising an emitter (source) connected to a power source line of a high level, a base (gate) connected to the external input terminal and a collector (drain) configured to be a first output terminal of a first control output;

an N-type transistor comprising an emitter (source) connected to a power source line of a low level, a base (gate) connected to the external input terminal and a collector (drain) configured to be a second output terminal of a second control output; ~~The decoder circuit according to claim 1, further comprising:~~

a voltage decreasing device one end of which is connected to the external input terminal; and

a first additional transistor comprising a base (gate) connected to another end of the voltage decreasing device or to a connection point of the voltage decreasing device, an emitter (source) connected to the power source line of the high level or the low level, and a collector (drain) configured to be a third output terminal of a third control output.

3. (Currently Amended) The decoder circuit according to claim [[1]] 2, further comprising:

a first voltage-dividing circuit connecting the external input terminal and the base (gate) of the P-type transistor and comprising four or more voltage-dividing resistors connected in series between the power source lines,

wherein the external input terminal is connected to a first connection point of the voltage-dividing resistors, the base (gate) of the P-type transistor is connected via a bias resistor to a second connection point of the voltage-dividing resistors, and the base (gate) of the N-type transistor is connected via a bias resistor to a third connection point of the voltage-dividing resistors, the second connection point is at a voltage level higher than the first connection point, and the third connection point is at a voltage level lower than the first connection point;

a first additional transistor comprising a base (gate) connected via a bias resistor to a connection point of the voltage-dividing resistors at a voltage level lower than the first connection point;

a second voltage-dividing circuit to which a current from the P-type transistor is supplied; and

a second additional transistor comprising a base (gate) connected via a bias resistor to a connection point of voltage-dividing resistors of the second voltage-dividing circuit.

4. (Currently Amended) A photo-detecting amplifier circuit for a disk recording/reproducing apparatus, being capable of switch function by means of a decoder circuit, the photo-detecting amplifier comprising:

a decoder circuit, mounted on an integrated circuit, comprising a P-type transistor, ~~and~~ an N-type transistor, a voltage decreasing device and a first additional transistor, wherein the decoder circuit decodes an input voltage supplied to a single external input terminal into three or more control outputs and generates[[ing]] a first control output, ~~and~~ a second control output and a third control output; and

an amplifier receiving the first and second control outputs

wherein the P-type transistor comprises an emitter (source) connected to a power source line of a high level, a base (gate) connected to the external input terminal and a

collector (drain) configured to be a first output terminal of [[a]] the first control output, and the N-type transistor comprises an emitter (source) connected to a power source line of a low level, a base (gate) connected to the external input terminal and a collector (drain) configured to be a second output terminal of [[a]] the second control output[[.]],

wherein one end of the voltage decreasing device is connected to the external input terminal, and

wherein the first additional transistor comprises a base (gate) connected to another end of the voltage decreasing device or to a connection point of the voltage decreasing device, an emitter (source) connected to the power source line of the high level or the low level, and a collector (drain) configured to be a third output terminal of the third control output.

5. (Currently Amended) An optical pickup including a photo-detecting amplifier circuit for a disk recording/reproducing apparatus, being capable of switch function by means of a decoder circuit, the optical pickup comprising:

a decoder circuit, mounted on an integrated circuit, comprising a P-type transistor, ~~and~~ an N-type transistor, a voltage decreasing device and a first additional transistor, wherein the decoder circuit decodes an input voltage supplied to a single external input terminal into three or more control outputs and generates[[ing]] a first control output, ~~and~~ a second control output and a third control output;

an amplifier receiving the first and second control outputs and generating signals; and

an optical element responsive to one of the signals generated by the amplifier,

wherein the P-type transistor comprises an emitter (source) connected to a power source line of a high level, a base (gate) connected to the external input terminal and a collector (drain) configured to be a first output terminal of [[a]] the first control output, and the N-type transistor comprises an emitter (source) connected to a power source line of a low

level, a base (gate) connected to the external input terminal and a collector (drain) configured to be a second output terminal of [[a]] the second control output[[.]],

wherein one end of the voltage decreasing device is connected to the external input terminal, and

wherein the first additional transistor comprises a base (gate) connected to another end of the voltage decreasing device or to a connection point of the voltage decreasing device, an emitter (source) connected to the power source line of the high level or the low level, and a collector (drain) configured to be a third output terminal of the third control output.